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APPLICATION FOR U.S. LETTERS PATENT

Title:

A Direct Digital Frequency modulation / Phase modulation decoder

In filing this non-provisional application, I claim the benefit of the filing date of Provisional Application Number 60/421,859 which I filed on 29 October 2002 and which bears the same title (under 35 U.S.C. § 119(e))

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Field of the invention

The present invention relates generally to signal demodulators, and particularly to decoders of Phase and Frequency modulations.

Background of the invention

Phase and frequency modulations are widely used in communication, and the decoding of such modulated signals has been the subject of many articles and inventions.

In phase modulation, the instantaneous phase deviation of the modulated signal from its unmodulated value is proportional to the instantaneous amplitude of the modulating signal. For a general modulating signal $v_m(t)$, the instantaneous phase deviation is, $\Theta(t)=k_\Theta v_m(t)$, wherein k_Θ is the phase deviation constant in radians per volts. For V_m defined as the maximum value of $|v_m(t)|$, it is convenient to define a "normalized" $v(t)=[v_m(t)]/V_m$, and in this notation, $\Theta(t)=k_\Theta V_m v(t)$, and the maximum phase shift, $k_\Theta V_m=\Delta\Theta=m_p$ is called the modulation index for phase modulation.

In terms of m_p the phase modulated signal is written as $F_{pm}(t)=A\cos[\omega_c t+m_p v(t)]$, and the instantaneous phase deviation is $\Theta(t)= m_p v(t)$, radians.

The instantaneous frequency of the modulated signal is $\omega(t) = \omega_c + \frac{d\Theta(t)}{dt} = \omega_c + m_p \frac{dv(t)}{dt}$.

Frequency modulation results when the deviation $\delta\omega$ of the instantaneous frequency $\omega(t)$ from the carrier frequency ω_c is directly proportional to the instantaneous amplitude of the modulating voltage.

Since $\omega(t) = \frac{d\phi}{dt} = \omega_c + \frac{d\Theta(t)}{dt}$ the frequency deviation $\delta\omega$ of $\omega(t)$ from ω_c is given by

$$\delta\omega(t) = \omega(t) - \omega_c = \frac{d\Theta(t)}{dt}.$$

In frequency modulation $\delta\omega(t)$ is proportional to the modulating voltage $v_m(t)$, as $\delta\omega(t)=k_m\, v_m(t)$, in which k_m is the sensitivity of the modulator in *rad/s/V*. Since $\Theta(t)$, and $\delta\omega(t)$ are related, as shown above, then $\Theta(t) = \int_0^t k_m v_m(t)dt + \Theta(0)$, and assuming $\Theta(0)=0$,

And $F_{FM} = A\cos\left[\omega_c t + k_m \int_0^t v_m(t)dt\right]$.

Demodulators of Phase and Frequency modulated signals, are used to extract the modulating signal $v_m(t)$ from the modulated signal. Such demodulators typically comprise of tuned circuits, or phase locked loops, in which a phase or frequency deviation causes a change in the output voltage, which is directly related to the magnitude of the phase or frequency deviation.

A simple FM demodulator is based on an LC tank resonator circuit. In resonance the amplitude versus the frequency response of the tuned circuit has the shape of a bell, as shown in figure 1. The LC tank is tuned to resonate, such that the center frequency (carrier frequency) of the FM modulated signal, and therefore any change in the signal frequency causes a change in the voltage on the resonator.

Figure 2, shows the most commonly used FM demodulator. To analyze this circuit, consider the voltage relationship in the coupled circuit *L1C1 – L2C2,* in figure 2, and figure 3. If the impedance coupled into the primary circuit is negligible in comparison with the primary self impedance, then the primary current I_1 will be

$$I_1 = \frac{V_1}{j\omega L_1}$$

The voltage induced in the secondary by I_1 is $j\omega M I_1$; at the secondary resonance frequency ω_c the secondary current will be:

$$I_2 = \frac{j\omega_c M I_1}{R_2} = \frac{M}{L_1}\frac{V_1}{R_2}$$

The voltage across the capacitor is: $2V_2 = j\omega_c C_2 I_2$, and therefore

$$V_2 = \frac{j\omega_c C_2 M}{2L_1 R_2} V_1$$

At resonance V_2 leads V_1 by 90°. At frequency ω slightly different from ω_c,

$$V_2 = \frac{j\omega C_2 M}{2L_1 R_2} \times \frac{V_1}{1+\left(1/R_2\right)\left[j\omega L_2 + \left(1/j\omega C_2\right)\right]} \approx$$

$$\approx \frac{j\omega C_2 M V_1}{2L_1 R_2} \times \left\{1 - \frac{1}{R_2}\left[j\omega L_2 + \frac{1}{j\omega C_2}\right]\right\}$$

and the phase angle between V_1 and V_2 is given by:

$$Arg\left(\frac{V_2}{V_1}\right) = Arg\left(j + \frac{\omega L_2}{R_2} - \frac{1}{j\omega C_2 R_2}\right) = \cot^{-1}\left(\frac{\omega L_2}{R_2} - \frac{1}{\omega C_2 R_2}\right)$$

Then, if $\omega = \omega_c + \Delta\omega$, the phase angle formula is reduced to

$$Arg\left(\frac{V_2}{V_1}\right) = \cot^{-1}\left(\frac{\Delta\omega L_2}{R_2}\right) = \cot^{-1}\left(\frac{\Delta\omega Q}{\omega_c}\right)$$ wherein $Q = \frac{\omega L_2}{R_2}$ which is the Q of the secondary resonant circuit.

For $\Delta\omega>0$, if $\omega>\omega_c$ then the angle is $<90°$, and if $\omega<\omega_c$ then the angle is $>90°$, as shown in figure 4.

Referring to figure 2, assuming that C_o and C_c are RF shorts, and that RFC is an RF open, the point "A" in figure 2, may be considered RF ground, and the RF voltage V_a' applied to the top diode, and the R_oC_o network is $V_a'=V_1+V_2$. The RF voltage V_b' applied to the bottom diode is $V_b'=V_1-V_2$. The phase relationship between V_1 and V_2 is shown in figure 4.

Figure 5, illustrates the variation of V_a', and V_b' as a function of variations in frequency. The basic relationships are:

$V_a'= V_b'$ when $\omega=\omega_c$,

$|V_a'|<|V_b'|$ when $\omega<\omega_c$,

$V_a'|>|V_b'|$ when $\omega>\omega_c$.

The demodulated output from the FM demodulator is $V_d=|V_a'|-|V_b'|$.
Since the phase deviation is the derivative of the frequency modulation, the phase demodulation is obtained by differentiating the frequency demodulator output.

An alternative method of FM demodulation, uses Phase Locked Loops (PLL), as the means to track frequency and phase deviations, and extract the modulating signal.

Referring to figure 6, showing a typical phase locked loop, comprised of a phase / frequency detector (61), a loop filter (62), and a voltage controlled oscillator (63). The control mechanism of the loop tries to maintain the loop in the locked state, wherein the signal at the output of the VCO (65) matches the phase and frequency of the reference input (66). As the reference input (66), which is the modulated signal, changes its phase or frequency, the loop follows those changes in order to stay locked. The voltage output of the loop filter (64) is directly proportional to the modulating signal.

In this invention, some new, completely digital, decoders for phase and frequency modulated signals are described. These decoders do not contain any tuned circuits, nor do they employ any phase locked loops. These decoders are inherently wideband, and the bandwidth of their operation is determined mainly by the frequency of the clock signal used.

This invention uses a direct phase sampler (DPS) to provide numerical information identifying the instantaneous phase of the input signal. Figure 7, shows a block diagram of a direct phase sampler. The DPS receives the modulated RF signal at its input, and on each clock transition it produces a digital number, indicating the instantaneous phase of the input signal at the time of the clock transition. Such phase samplers have been described before in other patens, and is not the subject of this invention.

Referring to figure 8, which shows a block diagram of an embodiment of a PM demodulator. The output of the DPS (100) is applied to a differencing circuit (10), which subtracts the phase of the input signal at the time of the last clock transition, from the phase of the input signal at the time of the previous clock transition, thus providing the phase difference between any two clocks. The output of the differencing circuit is applied both to a "p" deep running averager (20), and to the "A" input of a subtractor (30). The averager calculates the average of phase differences over the last consecutive "p" clock periods. The requirement on the averager length is that if t_c is the sampling clock period, and $t_{m(max)}$ is the period of the lowest frequency in the PM modulating bandwidth, then

$$p > 10\frac{t_{m(\max)}}{t_c}$$

The subtractor (30) , which follows the averager (20), subtracts the average phase difference calculated by the averager, from the instantaneous phase difference calculated by the differencing circuit. The resulting output is the variation in phase difference from clock transition to clock transition. A sine lookup table (40), which follows the subtractor (30), converts the phase variations information generated by the subtractor (30), into an amplitude voltage output (45), which is essentially the demodulation of the PM modulated input signal.

Figure 10, shows a block diagram of an FM demodulator. This demodulator is very similar to the PM demodulator, except that the output of the differencing circuit (10) is not applied directly to the "A" input of the subtractor (30), but instead is connected to a "q" deep running averager (50), who's output connects to the "A" input of the subtractor (30). The requirements for the size of "q" depend on the application. In general, "q" is much smaller than "p". However, the size of "q"

effects the decoder sensitivity, and its fidelity or linearity. The smaller "q" is, the higher is the demodulator's sensitivity, but the lower is its fidelity.

Description of the drawings

Figure 1, shows the amplitude versus frequency response of an LC tank resonator circuit.
Figure 2, shows the schematic of a typical "analog" frequency discriminator.

Figure 3, shows a circuit to illustrate the phase relationship in the discriminator. The resistors represent the internal resistance of the inductors.

Figure 4, shows the phase relationship in the discriminator.

Figure 5 shows the voltages on the diodes in the discriminator.

Figure 6, shows a Phase Locked Loop FM / PM discriminator.

Figure 7, shows a block diagram of direct digital phase sampler.

Figure 8, shows a block diagram of a direct digital PM demodulator.

Figure 9, shows an embodiment of a PM demodulator.

Figure 10, shows a block diagram of an FM demodulator.

Figure 11, shows an embodiment of an FM demodulator.

Figure 12, shows an embodiment of a receiver comprising a direct digital demodulator.

Figure 13, shows the waveforms involved in binary to Grey code conversion.

Figure 14, shows an embodiment of a phase to amplitude converter.

Figure 15, shows waveforms involved with phase to amplitude conversion.

Description of the invention

Figure 9, shows the details of an embodiment of a PM demodulator. The register (12), the subtractor (13), and the register (14), comprise the phase differencing circuit (10). The output of the direct digital phase sampler (101) $\Theta_k(t)$ is applied simultaneously to the input of the register (12), and the "A" input of the subtractor (13). The output of the register (13) lags behind the input to that register by one clock period, and thus the input "B" to the subtractor (13) $\Theta_{k-1}(t)$ lags one clock period behind the input "A" to the subtractor (13) $\Theta_k(t)$. As a result, the output of the subtractor (13), which is the difference between inputs "A" and "B" $\Delta\Theta_k=\Theta_k(t)-\Theta_{k-1}(t)$, is actually the change in the phase of the input signal (102), over one clock period, which is the instantaneous frequency of the input signal (102).

The adder (21), the "p" deep shift register (22), the register (23), the subtractor (24), and the register (25), comprise the averager (20). Assuming that initially all registers and shift registers outputs are "0". The output of the shift register (22) will remain "0" for at least "p" clock cycles, as any non "0" data at the input to the shift register (22) propagates through the shift register in "p" clock periods. The adder (21) adds new data $\Delta\Theta_k$ coming from the differencing circuit (10) [register (14)], with data Φ_k coming out of the subtractor (24) via the register (25). While the output of the shift register (22) $\Delta\Theta_{k-p}$ is "0" for "p" clock cycles, the output of the subtractor (24) $\Phi_k=\Lambda_k-\Delta\Theta_{k-p}$ is the same as the data at its "B" input Λ_k. As a result, for the first "p" clock cycles, the adder (21) accumulates all the phase differences generated by the subtractor (13) $\Lambda_{k+1}=\Phi_k+\Delta\Theta_k=\Lambda_k-\Delta\Theta_{k-p}+\Delta\Theta_k$. The divider (26), which follows the register (25) divides the output from the subtractor Φ_k by p, to yield the running average $\Delta\Theta_{AVG}=\frac{\Sigma(\Delta\Theta_k-\Delta\Theta_{k-p})}{p}$. If p is selected such that $p=2^n$, then the division can be accomplished by simply discarding the n least significant bits at the output of the averager. The output of the averager is the average phase difference for any clock period. Dividing the average phase difference by the clock period yields the average, or center frequency of the input signal $F_c=\frac{\Delta\Theta_{AVG}}{t_c}$.

The output of the averager (20) $\Delta\Theta_{AVG}$ is subtracted by the subtractor (31) from the instantaneous phase difference $\Delta\Theta_k$ to yield the phase deviation $\theta_k=\Delta\Theta_{AVG}-\Delta\Theta_k$.

A sine lookup table (41) followed by a digital to analog converter (42), is a convenient way to convert phase information to amplitude information for the demodulator output.

Figure 11, shows an embodiment of an FM demodulator. This demodulator is very similar to the PM demodulator. It uses the same phase sampler (101), the same differencing circuit (10), the same averager (20), the same subtractor (30) and the same sine lookup table (40). The only difference is that the input "A" of the subtractor (31) is not connected to $\Delta\Theta_k$, the output of the differencing circuit (10), but instead, an averager (50), which is comprised of the subtractor (51), q deep shift register (52), register (53), subtractor (54), register (55), and divider (56). The operation of this averager (50), is similar to the operation of the averager (20), with the only difference in the length of the shift register which is q<<p.

In the FM demodulator, the averager (50), having a shift register much shorter than that of the other averager (20), produces the instantaneous deviated frequency $F_d = \frac{\Delta\Xi_{AVG}}{t_c}$, wherein $\Delta\Xi_{AVG}$ is the average phase difference per clock period output of the averager (50). The subtractor (31) subtracts the instantaneous deviated frequency from the center frequency, resulting in the frequency deviation $\Delta F=F_d-F_c$, The sine lookup table (40) converts the phase information into amplitude information, to complete the demodulation process.

An alternative method and circuit for converting phase information into voltage amplitude is shown in figures 13, 14, and 15.

In digital presentation of numbers the bits are assigned values which are power of 2 wherein the least significant bit is assigned the value of 2^0, the next bit is 2^1, etc. In binary code presentation the order of values in 4 bits is: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15. In a Grey code on the other hand, the order of values is: 0,1,3,2,6,7,5,4,12,13,15,14,10,11,9,8. When these values are presented in 4 bits waveforms, the resulting Grey code waveforms are symmetrical, unlike the binary code, which is non-symmetrical. This symmetry feature of Grey code waveforms enables their use in phase to amplitude conversion.

Obtaining Grey code out of binary code is a straight forward process of EXORing pairs of bits in the form $G_n = B_n \oplus B_{n+1}$. The most significant bit (MSB) in the Grey code is the same as the MSB in binary code, as shown in figure 13.

Figure 14, shows an embodiment of a phase to amplitude converter. Following the conversion of binary to Grey code (1), the Grey code bits are further EXORed (2) and applied to amplifiers with output spanning between a positive supply rail (+V) to a negative supply rail (-V). The resulting

voltage waveforms are applied to a resistive network (3). In the resistive network, currents are summed together on the output resistor (R(out)) to generate a sinewave approximation waveform output (4). Figure 15, shows the waveforms in converting phase information presented in Grey code into a sinewave approximation waveform.

Figure 12, shows an embodiment of a receiver utilizing a digital demodulator. The input signal (212) is split in the power splitter (201) into two equal but lower power version of the input signal. These signals are applied to two RF mixers (203, and 204). A local oscillator (211) generates a signal, at a frequency which when added to (or subtracted from) the input signal (212) yield a frequency which is in the center of the band of the bandpass filters (204). The output of the oscillator is passed through a Hybrid Coupler (202), which splits the oscillator's output into two signals with equal amplitudes but with a 90° phase relationship. The two signals generated by the hybrid coupler (202) are applied to the mixers (203, and 204) at their LO ports. As a result, the mixers (203, and 204) outputs are two signals at a frequency of the center of the bandpass filters, and with a 90° phase relationship between them. These signals pass through the bandpass filters, and are applied to the direct phase digitizer as "I" and "Q" (209, and 210 respectively). The digital processing is operating with a clock (not shown). On every clock cycle, the digitizer (206) generates a data output representing the phase of the input signal at the time of the clock transition. The digital demodulator (207) receives the data output from the digitizer (206) and extracts the modulating signal from the modulated input signal (212).